METHOD OF FORMING A PARTIALLY DEPLETED SILICON ON INSULATOR (PDSOI) TRANSISTOR WITH A PAD LOCK BODY EXTENSION

BACKGROUND OF THE INVENTION

(1) Field of the Invention

The present invention relates to methods used to fabricate semiconductor devices, and more specifically to a method used suppress the effect of floating body regions used with metal oxide semiconductor field effect transistor (MOSFET) devices formed on an SOI layer.

(2) Description of Prior Art

The ability to form MOSFET devices, such as a partially depleted MOSFET device, on a silicon on insulator (SOI) layer has resulted in decreased junction capacitance and thus increased device performance. To avoid a body floating phenomena which can result in deleterious device characteristics such as a low source to drain breakdown voltage, as well as threshold voltage reduction, direct contact between the semiconductor substrate and a body contact region, formed in the SOI layer, is employed. However designs using a body contact region of a first conductivity type can form unwanted parasitic transistor with source and drain regions of a second conductivity type, in an area adjacent to, or underlying the gate structure of the MOSFET device. The leakage current resulting from the unwanted parasitic transistors can negatively

influence the performance of the MOSFET device.

The present invention will describe a structure, as well as a process used to fabricate this structure, that reduces the leakage current driven by the parasitic transistors that can form at a gate electrode junction. The same structure in addition to reducing leakage current of unwanted parasitic transistors, also allows greater control of gate width to be realized. Prior art such as Kroell et al in U.S. Pat. No. 6,537,861 B1, Beyer et al in U.S. Pat. No. 5,405,795, Kim et al in U.S. Pat. No. 6,521,959 B2, and Tyson et al in U.S. Pat. No. 5,145,802, describe methods of forming body extension and body contact regions, however these prior art do not describe the structure and process used in this present invention which features the reduction of the deleterious leakage current generated by the presence of the body contact region via inclusion of novel isolation regions.

SUMMARY OF THE INVENTION

It is an object of this invention to fabricate a MOSFET device in a SOI layer employing body contact regions formed in the same SOI layer.

It is another object of this invention to form shallow trench isolation (STI) regions in the SOI layer, with the STI regions located underlying a portion of a gate structure in turn located between the body contact region and adjacent MOSFET source/drain regions, to eliminate parasitic transistor formation at the junction of the gate structure and body contact region.

It is still another object of this invention to employ STI regions between body contact regions and specific elements of a MOSFET device, wherein the STI regions are underlying portions of "T" shaped , as well portions of "H" shaped conductive gate structures.

In accordance with the present invention a MOSFET device structure, and a process used to fabricate said MOSFET device structure, featuring STI regions placed at specific locations of the MOSFET device, and used to eliminate parasitic transistor formation at the junction of the MOSFET regions, is described. Before growth of a gate insulator layer on a silicon on insulator (SOI) layer, insulator filled STI regions are formed in the SOI layer, with the depth of the STI region equal to the thickness of the SOI layer. "T" shape or "H" shape conductive gate structures are next defined on the underlying gate insulator layer and on portions of the STI regions. A body contact region featuring the same conductivity type as the semiconductor substrate is next formed in an non-active region of the SOI layer, adjacent to a component of the conductive gate structure and butting the STI region. Source/drain regions are then formed in portions of the active device regions of the SOI layer not covered by the conductive gate structure, with the source /drain regions located adjacent to the same conductive gate structure component, and butting the opposite side of the same STI region.

BRIEF DESCRIPTION OF THE DRAWINGS

The object and other advantages of this invention are best described in the preferred embodiment with reference to the attached drawings that include:

Figs. 1B, 2B, 2C, 3B, 4B and 5B, which schematically in cross-sectional style describe key stages used to fabricate a MOSFET device featuring STI regions formed to eliminate parasitic transistor formation at the junction of the MOSFET gate structure and a body contact region.

Figs. 1A - 5A, which schematically show top views of the MOSFET device structure, comprised with STI regions located at the junction of the gate structure and body contact region, at various stages of fabrication.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

The method of fabricating a MOSFET structure featuring STI regions formed at specific locations of the MOSFET device, to reduce parasitic transistor formation at the junction of a MOSFET device region and a body contact region underlying a conductive gate structure, will now be described in detail. Semiconductor substrate 1, comprised of P type, single crystalline silicon featuring a <100> crystallographic orientation, is used and schematically shown in Fig. 1B. A silicon on insulator (SOI) layer comprised of silicon layer 3, on silicon oxide layer 2, is next formed on semiconductor substrate 1, via a SIMOX (separation by implanted oxygen), procedure. The SIMOX procedure features implantation of oxygen ions into semiconductor substrate 1, followed by an anneal procedure resulting in a buried silicon oxide layer 2, at a thickness between about 1000 to 3000 Angstroms, and overlying, the non-implanted top portion of semiconductor substrate 1, now defined as silicon layer 3, at a thickness between about 1000 to 3000 Angstroms. If desired the SOI configuration can also be obtained via bonding of a first

silicon oxide layer located on a first semiconductor substrate, to an second silicon oxide layer located on a second semiconductor substrate. Removal of semiconductor material from semiconductor substrate, to a point in which the thinned semiconductor substrate is now the silicon layer of the SOI configuration, is then accomplished via a chemical mechanical polishing (CMP) procedure. Photolithographic and dry etching procedures are next used to selectively define the desired configuration of silicon shape 3, overlying insulator layer 2. Removal of the photoresist shape used for definition of silicon layer, or silicon shape 3, is accomplished via plasma oxygen ashing procedures.

To reduce the risk of parasitic transistor formation at specific regions of the MOSFET device insulator filled, shallow trench isolation (STI), regions 4, are formed at the specific locations in which subsequent parasitic transistor formation can result. Photolithographic and reactive ion etching (RIE), procedures are used to define shallow trench shapes in silicon layer 3, using Cl_2 as a selective etchant for silicon. The selective RIE procedure terminates at the appearance of insulator layer 2. The area of the shallow trench shapes is maintained small, defined with an area between about 2Lg x 2Lg to 10Lg x 10Lg um^2, (wherein Lg is equal to gate length), to minimize hot carrier generation. An insulator layer such as silicon oxide is next deposited via low pressure chemical vapor deposition (LPCVD), or via plasma enhanced chemical vapor deposition (PECVD), procedures, completely filling the shallow trench shapes. Removal of portions of the shallow trench filling insulator layer from the top surface of silicon layer 3, is accomplished selectively via a CMP procedure, resulting in STI regions 4, in silicon layer 3. This is shown schematically in cross-sectional style in Fig. 1B, with the top view of the in-process

MOSFET device shown schematically as a top view in Fig. 1A. After formation of STI regions 4, gate insulator layer 10, comprised of silicon dioxide is thermally grown to a thickness between about 10 to 100 Angstroms. This is shown schematically in Fig. 1B.

Formation of a conductive gate structure is next addressed and shown schematically in cross-sectional style using Figs. 2B and 2C, and shown as a top view using Fig. 2A. A conductive material such as polysilicon is deposited via LPCVD procedures at a thickness between about 1000 to 2000 Angstroms. The polysilicon layer can be doped in situ during deposition via the addition of arsine or phosphine to a silane or disilane ambient, or the polysilicon layer can be deposited intrinsically then doped via implantation of arsenic or phosphorous ions. Photolithographic and anisotropic RIE procedures, using Cl_2 as a selective etchant for polysilicon, are used to define polysilicon gate structure 5. If desired gate structure 5, can be comprised of a metal silicide layer such as tungsten silicide, or comprised of a composite featuring an overlying metal silicide component on an underlying polysilicon component. Fig. 2A, schematically shows a "T" shaped polysilicon gate structure with the width of the horizontal component of polysilicon gate structure 5, located in an active device region, between about 10 to 350 nm. This width will subsequently define the channel length of the MOSFET device. The vertical component of polysilicon gate structure 5, is defined overlying a portion of the top surface of STI region 4. Without the presence of STI region 4, subsequent formation of a body contact region in a non-device region of the MOSFET device in an area adjacent to a source/drain region could result in the creation of a parasitic transistor underlying the polysilicon gate structure 5, at the edge of the active device region. This unwanted result is avoided via formation of STI region 4, at the

specific location in which the parasitic transistor would be formed. In addition the presence of STI region 4, partially determines gate width, thus reducing the margin of photolithographic alignment error, resulting in improved greater gate width to be realized. The result of these procedures, shown schematically as a top view in Fig. 2A, is also shown in cross-sectional style in Fig. 2B. The active device region at this stage of fabrication is schematically shown in cross-sectional style in Fig. 2C.

A portion of silicon shape 3, located between shallow trench regions 4, will be used for will be used as body contact region 6, while remaining portions of silicon shape 3, not covered by polysilicon gate structure 5, will subsequently be used to accommodate MOSFET source/drain regions. This is schematically shown in cross-sectional style in Fig. 3B, and as a top view using Fig. 3A.

This invention can be used for both N channel (NMOS), devices, as well as for P channel (PMOS), devices. Description of an NMOS device featuring a body contact region and shallow trench isolation will be described below, however it should be understood that PMOS devices, or complimentary metal oxide semiconductor (CMOS), devices comprised of both NMOS and PMOS devices, can be fabricated using this invention. After removal of the photoresist shape used to define polysilicon gate structure 5, via plasma oxygen ashing and wet clean procedures, formation of either N type or P type regions in the device area of the MOSFET structure is addressed. A photoresist block out shape, not shown in the drawings, is used to protect a portion of a PMOS region (not shown in the drawings), from an N type ion implantation procedure used to form the heavily doped N type source/drain region of the NMOS device. Implantation of

arsenic or phosphorous ions is performed at an energy between about 5 to 40 KeV, at a dose between about 2E15 to 8E15 atoms/cm^2. The same N type ion implantation procedure is also applied to the portion of a PMOS device creating an N type body contact region for the PMOS device. After removal of the photoresist blockout shape via plasma oxygen ashing procedures, an anneal procedure is performed to activate the implanted N type ions, resulting in N type source/drain regions 7, in portions of silicon shape 3, not covered by polysilicon gate structure 5. In addition a heavily doped N type region is also formed in a top portion of body contact region 6. This is schematically shown in cross-sectional style in Fig. 4B, and shown as a top view in Fig. 4A. The identical process sequence is also employed for the formation of heavily doped P type source/drain regions for the PMOS device. That is photoresist block out of the NMOS region allowing a P type ion implantation procedure to form a heavily doped P type heavily doped source/drain region only in the PMOS device region. An N type body contact region had already been formed in the PMOS region during the ion implantation procedure used to form the N type heavily doped source/drain region for the NMOS device. This is not shown in the drawings.

The completion of the MOSFET device featuring STI regions 4, used to reduce the possible formation of a parasitic transistor at a junction underlying polysilicon gate structure is accomplished via formation of insulator spacers on the sides of polysilicon gate structure 5, as well as metal silicide formation on source/drain regions 7, body contact region 6, and on the top surface of polysilicon gate structure 5. These processes are not described in this application.

The inclusion of STI regions to reduce the risk of parasitic transistor formation at specific

regions of the MOSFET devices formed on SOI layers, shown for "T" shaped gate structures in the preceding description can also be applied to MOSFET devices formed on SOI layers, comprised with different gate structures, such as "H" shaped gate structures. The identical process sequence used to reduce parasitic transistor formation for the MOSFET device featuring a "T" shaped gate structure is again employed to fabricate a MOSFET device comprised with an "H" shaped gate structure. STI regions 4, are again formed in specific regions of the MOSFET device resulting in an active device region, or the channel width defined by the space between STI regions 6, while channel length is still defined by the width of the conductive gate structure 5. Parasitic transistor formation is reduced underlying the junction of the conductive gate structure components via the physical separation of body contact region 6, and source/drain regions 7, supplied by STI regions 4. This is schematically shown as a top view in Fig. 5A, and as a cross-sectional view in Fig. 5B.

While this invention has been particularly shown and described with reference to, the preferred embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made without departing from the spirit and scope of this invention.

What is claimed is: